CLAIMS

1. (Previously Presented) A bus architecture for a plurality of dedicated SRAM blocks in an FPGA comprising:

a plurality of pass-through interconnect conductors, each of said plurality of said pass-through interconnect conductors having a first end connected to one of said first plurality of programmable connectors and a second end connected to one of said second plurality of programmable connectors wherein said first plurality of programmable connectors are connected to FPGA routing conductors of a first edge of said FPGA and said second plurality of programmable connectors are connected to routing conductors of a second edge of said FPGA;

an address bus disposed in one of said plurality of dedicated SRAM blocks forming first intersections with said plurality of pass-through interconnect conductors;

a data bus disposed in one of said plurality of dedicated SRAM blocks forming second intersections with said plurality of pass-through interconnect conductors;

a control signal line disposed in one of said plurality of dedicated SRAM blocks forming third interconnect intersections with said plurality of pass-through interconnect conductors; and

programmable elements disposed at selected ones of said first, second and third intersections.